

FIG. 1

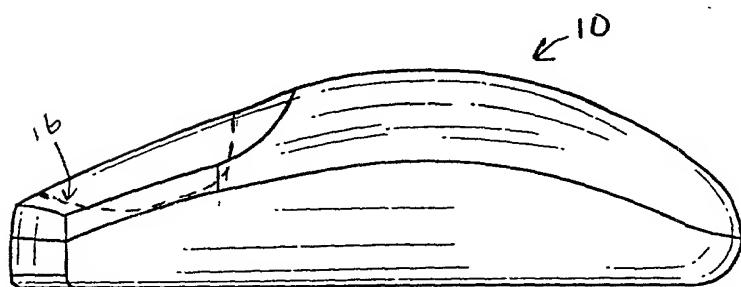


FIG. 2



FIG. 3

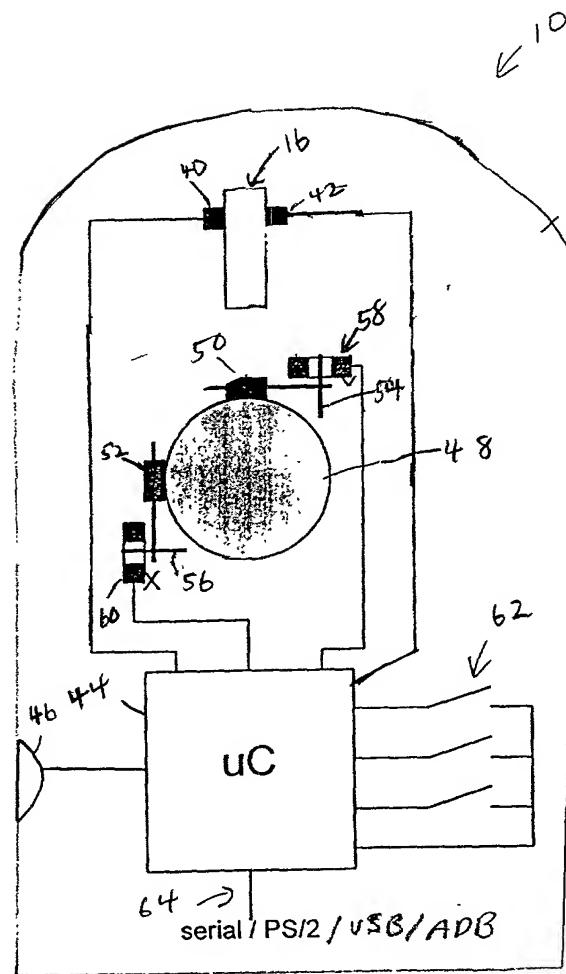


FIG. 4

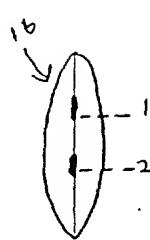


FIG. 5A

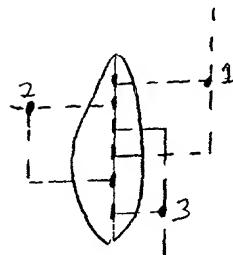


FIG. 5B

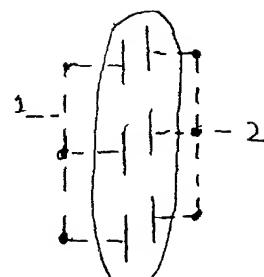


FIG. 5C

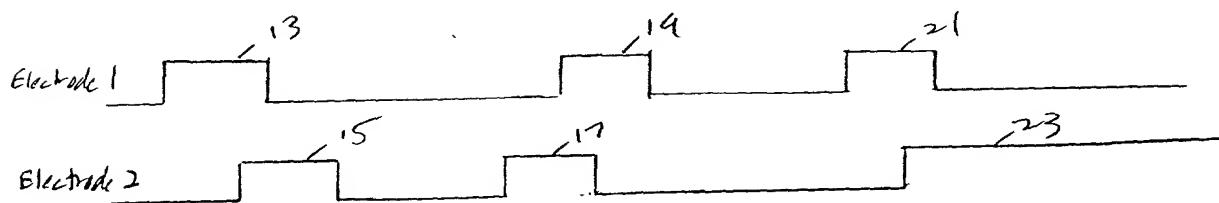


FIG. 5D

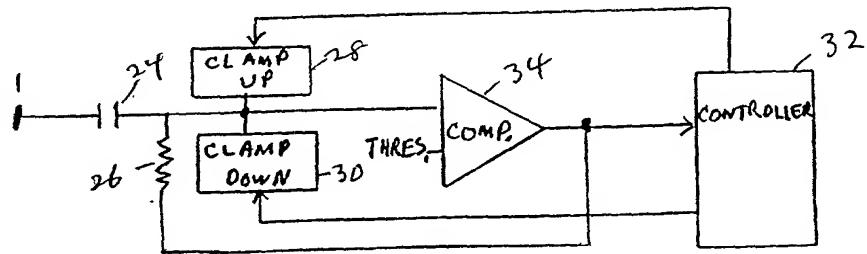


FIG. 6

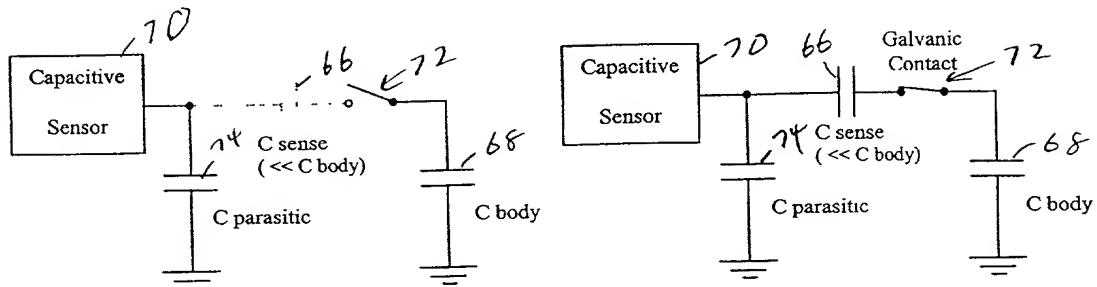


FIG. 7A

FIG. 7B

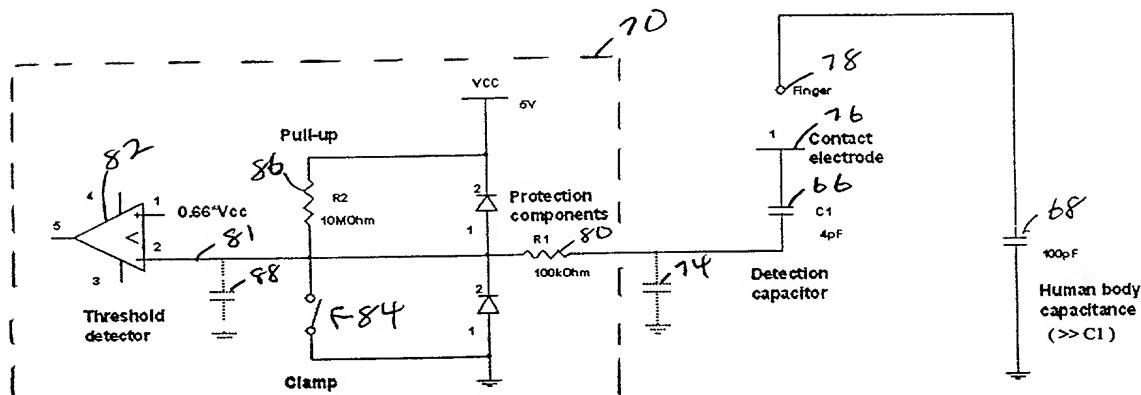


FIG. 8

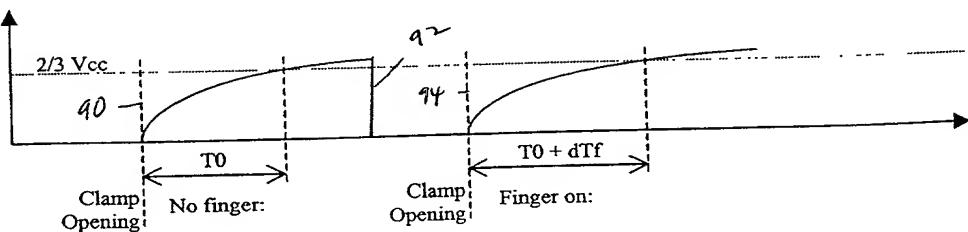


FIG. 9

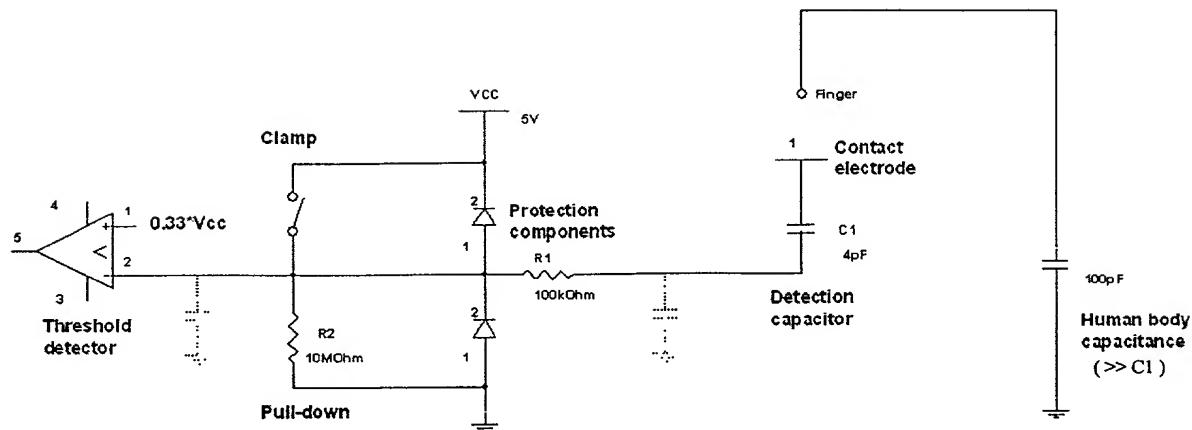


FIG. 10

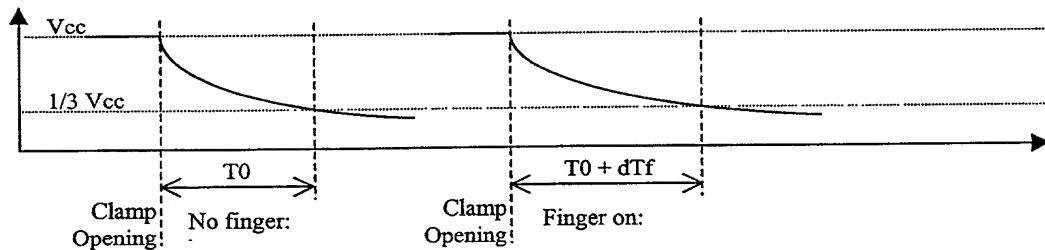


FIG. 11

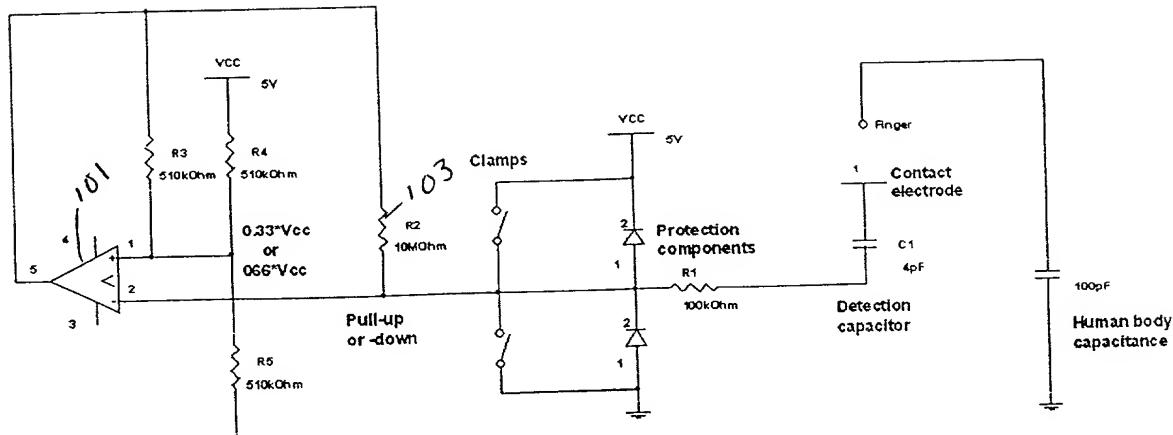


FIG. 12

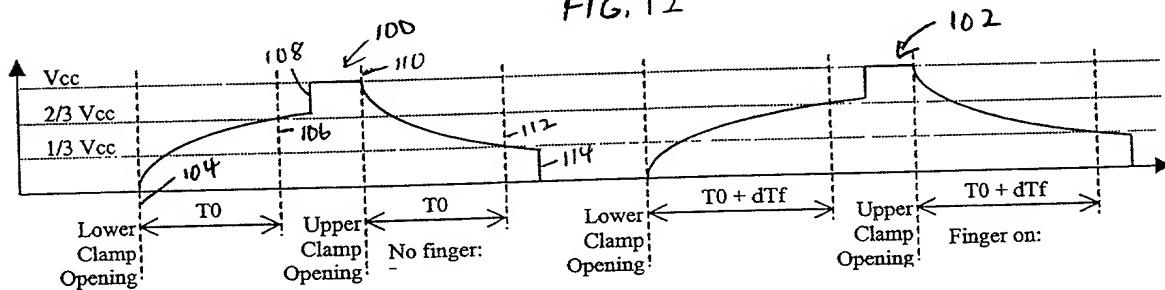


FIG. 13

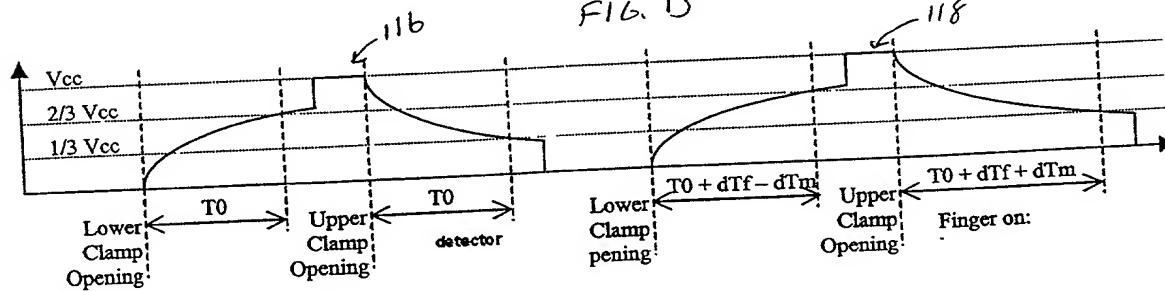


FIG. 14

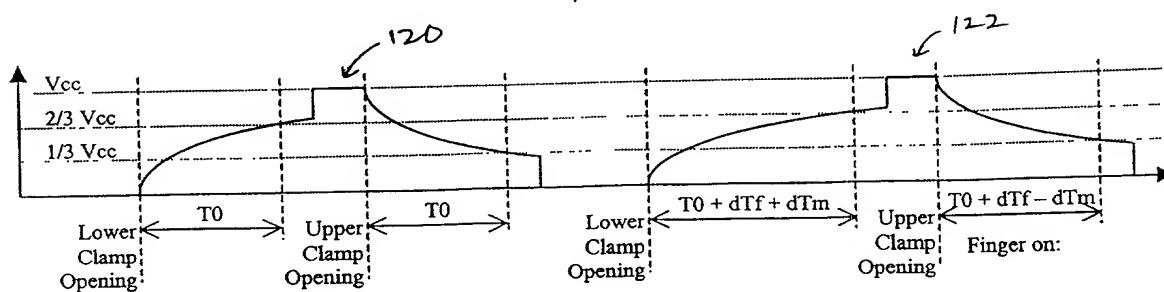
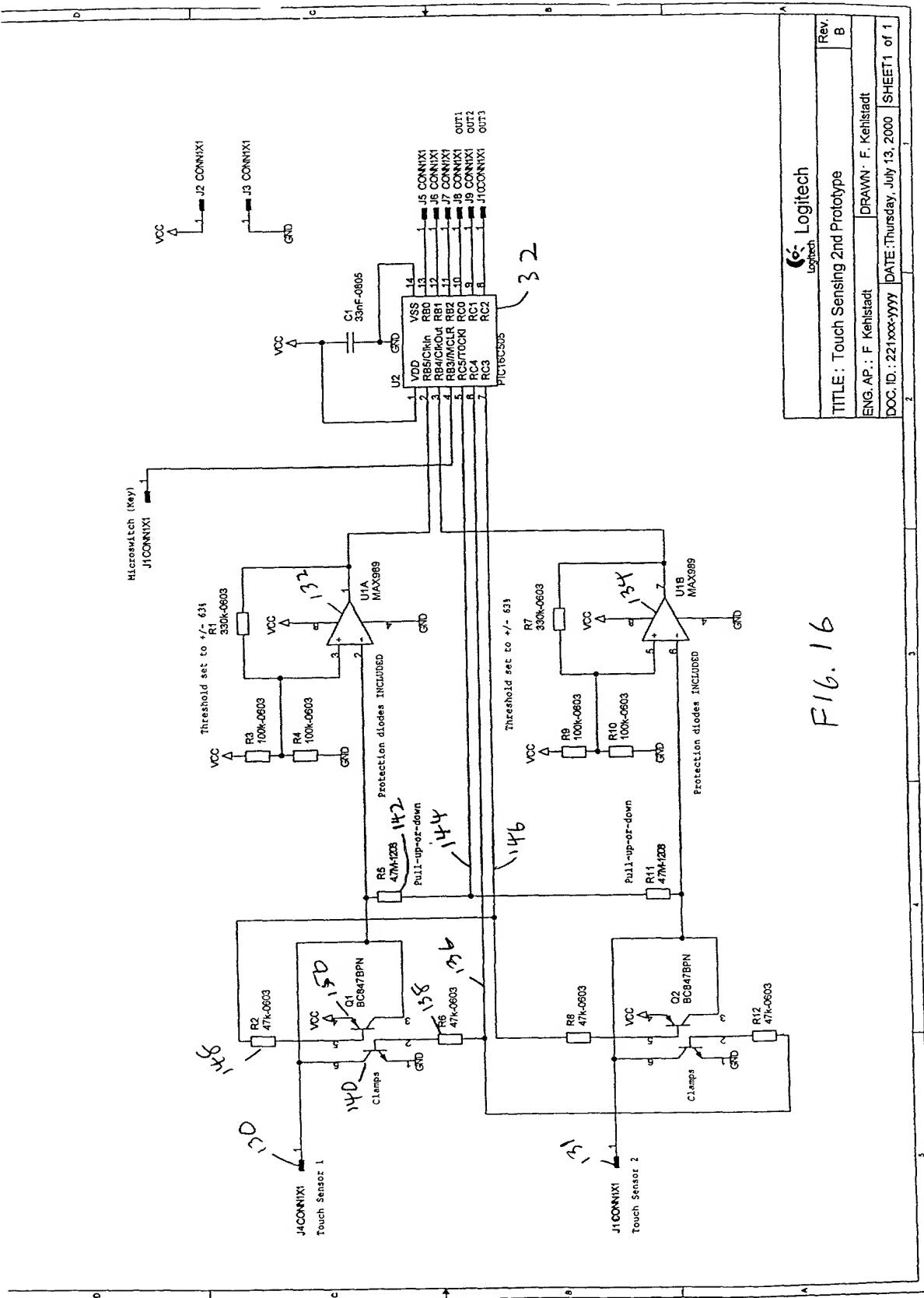


FIG. 15



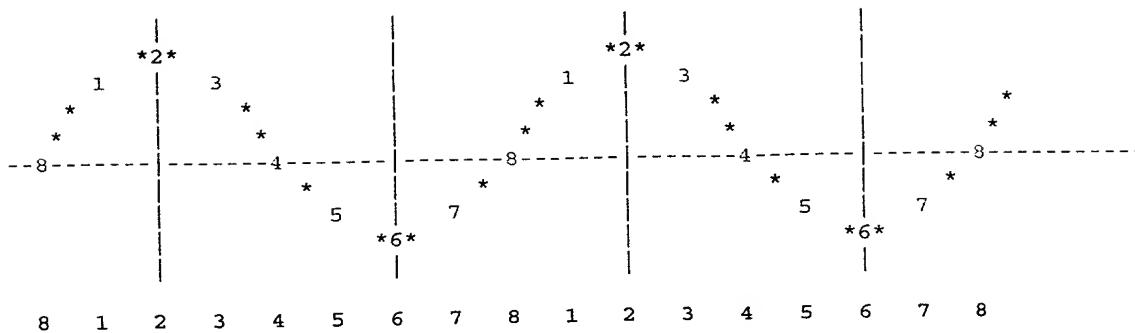


FIG. 17

4 0 0 2 5 6 3 6 4 2 1 3 0 4

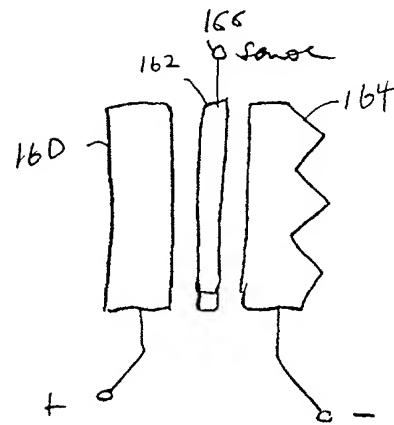


FIG. 18

FIG. 19 shows a circuit diagram with a central node labeled 162, which is labeled 'sense'. A capacitor labeled  $C_{p\infty}$  is connected between node 162 and a terminal labeled '+'. A capacitor labeled  $C_{1\infty}$  is connected between node 162 and a terminal labeled '−'. A capacitor labeled  $C_{2\infty}$  is connected between node 162 and a terminal labeled '−'. A capacitor labeled  $C_{3\infty}$  is connected between node 162 and a terminal labeled '−'. The equation for the equivalent capacitance is given as  $C_{\text{eq}} = \left( \frac{1}{C_1} + \frac{1}{C_2} \right)^{-1} = C_{\text{eq}}(x)$ .

FIG. 19

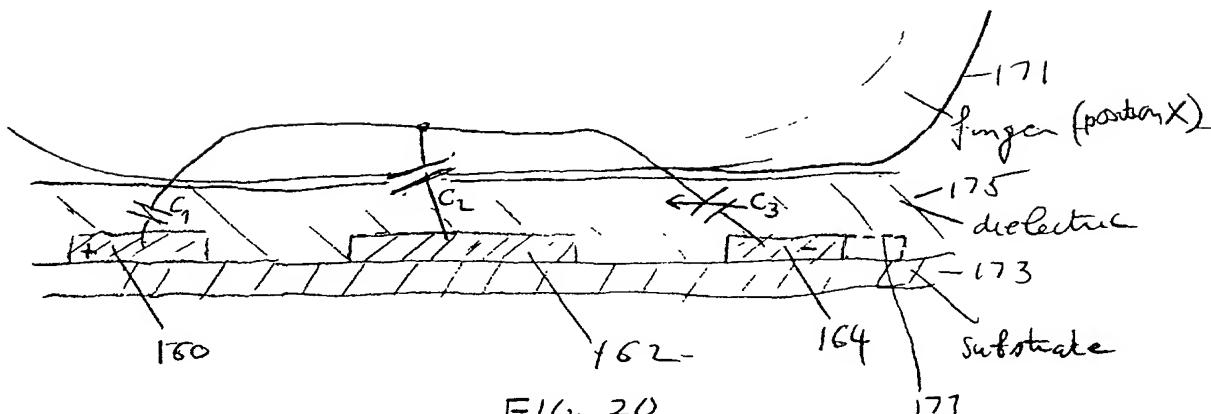
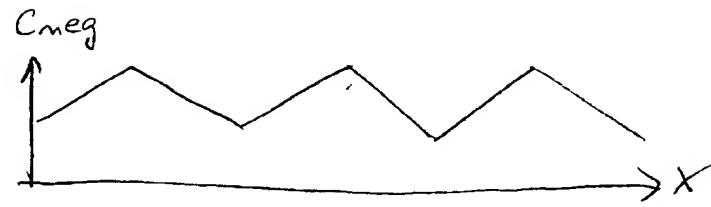


FIG. 20

10025336 - 423304

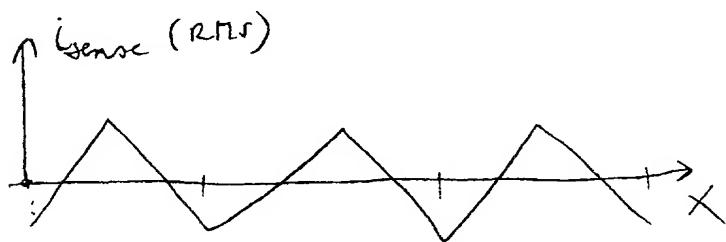
21 A



21 B



21 C



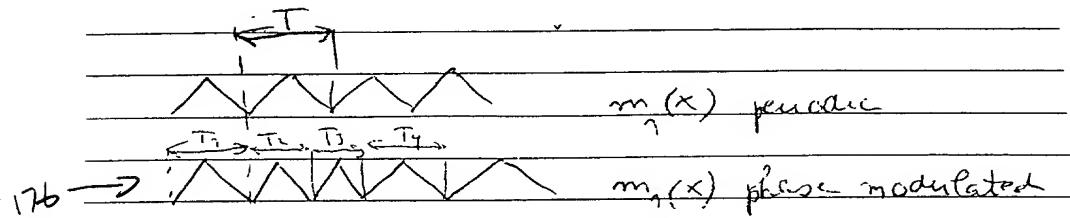


FIG. 22

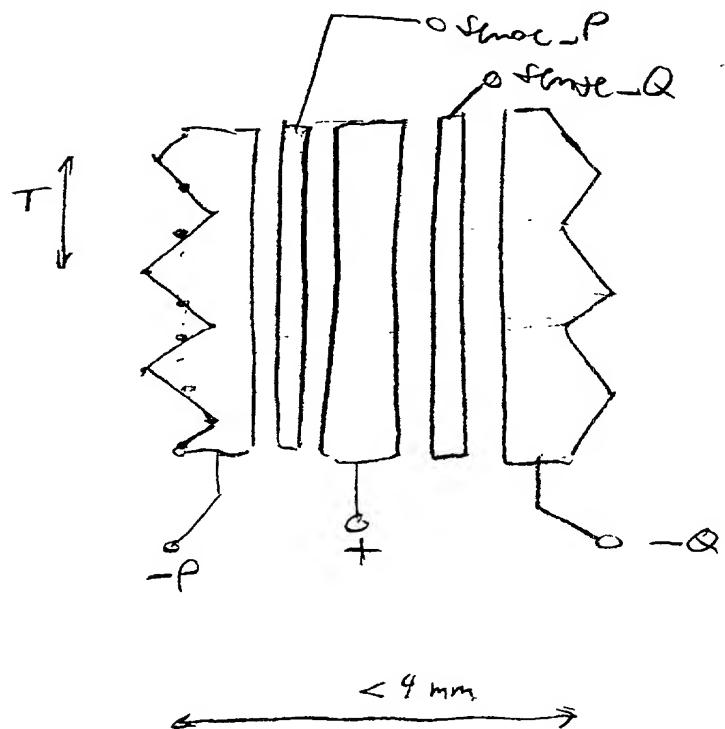


FIG. 23